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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,605	06/27/2003	Kong Weng Lee	70030259-1	2253

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AGILENT TECHNOLOGIES, INC.  
Legal Department, DL429  
Intellectual Property Administration  
P.O. Box 7599  
Loveland, CO 80537-0599

EXAMINER
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MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/608,605

Applicant(s)

LEE ET AL.

Examiner

Thomas J. Magee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections – 35 U.S.C. 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 6, 7, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wyland (US 5,986,885).

3. Regarding Claim 1, Wyland discloses a packaging device for semiconductor die, comprising:

a substantially planar substrate having opposed major surfaces (60) (Figure 6),  
a conductive “mounting pad” (61) located on one of the major surfaces,  
a conductive “connecting pad” (63) located on the other of the major surfaces, and  
a conductive interconnecting element (62) extending through the substrate (60) and electrically interconnecting the mounting pad (61) and connecting pad (63).

4. Regarding Claims 2 and 7, Wyland discloses (Col. 7, lines 22 – 25) that the substrate comprises ceramic.

5. Regarding Claims 4 and 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper.

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6. Regarding Claim 6, Wyland discloses the packaging device of Claim 1, additionally comprising:

- a bonding pad (right side, Figure 6) (31) (Col. 7, lines 19 – 21) located “on” one of the major surfaces,

- an additional conductive connecting pad (63, right side) located on the other of the major surfaces, and

- an additional conductive interconnecting element (62, right side) extending through the substrate and electrically interconnecting the bonding pad and the additional connecting pad.

7. Claims 11, 12, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (US 6,084,295).

8. Regarding Claim 11, Horiuchi et al. disclose a semiconductor device, comprising:

- a substantially planar substrate having opposed major surfaces (5) Figure 1),

- a conductive “mounting pad” (upper surface) (Figures 1, 7(a) and 7(c)) (Col. 6, line 64 – Col. 7, line 2) located on one of the major surfaces,

- a conductive connecting pad located on the other of the major surfaces Figures 1, 7(a) and 7(c)) (Col. 6, line 64 – Col. 7, line 2),

- a conductive interconnecting element (42) extending through the substrate and electrically connecting the mounting pad and the connecting pad (Col. 6, line 64 – Col. 7, line 2), and

- a semiconductor die (10) (Figure 1) attached to the mounting pad.

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9. Regarding Claims 12 and 18, Horiuchi et al. discloses (Col. 6, lines 1 – 3) that the substrate is ceramic.

10. Regarding Claim 16, the three claim elements are discussed in Claim 11. Further, Horiuchi et al. disclose a bonding wire (20) (Figure 1) extending between the semiconductor die (10) and the bonding pad.

11. Regarding Claim 17, Horiuchi et al. disclose that an encapsulant (34) (Figure 1) encapsulates the semiconductor die and at least a portion of the major surface of the substrate on which the mounting pad is located (Col. 5, lines 34 – 37).

### ***Claim Rejections – 35 U.S.C. 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 3 and 8 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Electronic Packaging and Production ("Innovative PCB Reinforcement," (February, 1997), p. 1).

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14. Regarding Claims 3 and 8, Wyland does not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5<sup>th</sup> para.).

15. Claims 5 and 10 are rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993), p. 868 – 872).

16. Regarding Claims 5 and 10, Wyland does not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

17. Claim 9 is rejected under 35 103(a) as being unpatentable over Wyland, as applied to Claims 1, 2, 4, 6, 7, and 10, and further in view of Moyer et al. (US 6,620,720 B1).

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18. Regarding Claim 9, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper, but does not disclose that the bond pad is composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

18. Claims 13 and 18 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Electronic Packaging and Production.

19. Regarding Claims 13 and 18, Horiuchi et al. do not disclose a substrate material composed of epoxy laminate. However, epoxy laminate substrates are well known and widely used in the art. Electronic Packaging and Production discloses (p. 1, middle column, bottom para.) that epoxy laminate substrates have been in use for almost a decade. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Horiuchi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5<sup>th</sup> para.).

20. Claims 15 and 20 are rejected under 35 103(a) as being unpatentable over Horiuchi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Wilson et al.

21. Regarding Claims 15 and 20, Horuichi et al. do not disclose a conductive interconnecting element (via) comprising tungsten. Wilson et al. disclose that conductive interconnect elements (vias) composed of tungsten are well established in the art (p.868, lines 7 – 12). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horuichi et al. to reduce costs (p. 868, lines 11 – 12) and reduce signal delays (p. 872, Figure 10).

22. Claim 19 is rejected under 35 103(a) as being unpatentable over Horuichi et al., as applied to Claims 11, 12, 16, and 17, and further in view of Moyer et al. and Wyland.

23. Regarding Claim 19, Horuichi et al. do not disclose that the mounting pad, bond pad, and connecting pad are composed of copper. However, Wyland discloses (Col. 7, lines 31 – 39) that the mounting pad (61), and the connecting pad (63) are composed of copper. Moyer et al. disclose (Col. 2, lines 48 – 49) that a copper contact (bond) pad (13) (Figure 1) is formed on the silicon substrate for either wire bonding or solder bump bonding. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horuichi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., Col. 1, lines 41 – 43).

### ***Conclusions***

24. Any inquiry concerning this communication or earlier communications from the



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Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a stylized, flowing script.

EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Thomas Magee  
August 15, 2004